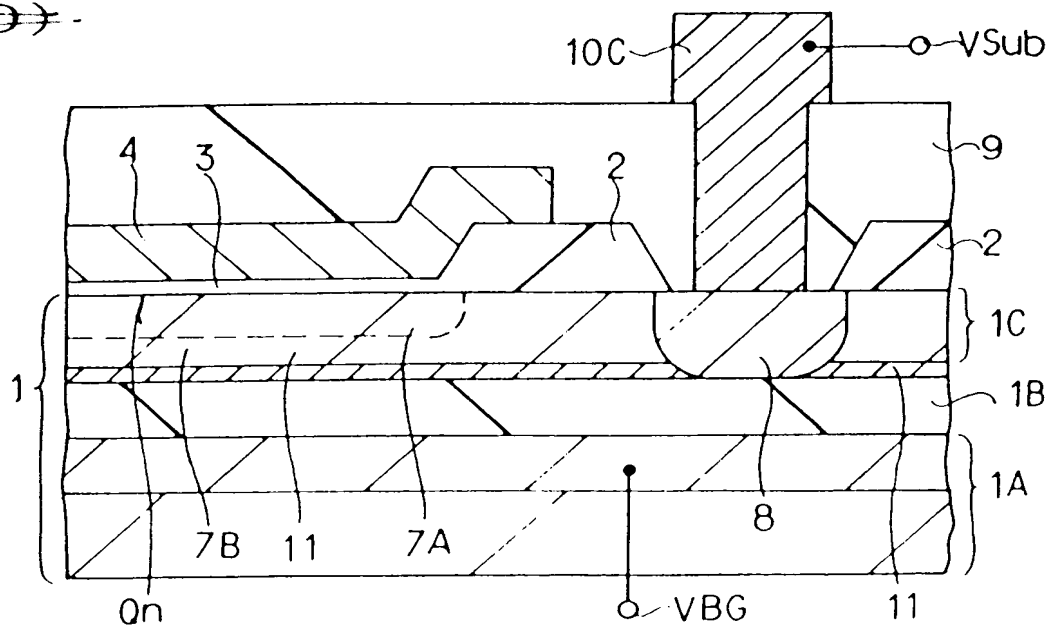


Figure A is a cross-sectional view of a semiconductor device. The structure consists of several layers and regions. At the top, there are two gate regions labeled 10A and 10B, which are connected to terminals VS and VDS, respectively. Between these gate regions is a central region labeled 7A. Below the gate regions, there are two side regions labeled 2 and 3, and a central region labeled 4. The bottom of the device features a series of horizontal layers labeled 1A, 1B, and 1C. A central region labeled 6 is located between the 1A and 1B layers. A terminal labeled VBG is connected to the bottom of the central region 6. A terminal labeled Qn is connected to the bottom of the central region 4. The entire structure is supported by a substrate labeled 1.

[illegible]

(C)

~~(D)~~ -

~~FIG. 5~~

FIG 5(A)

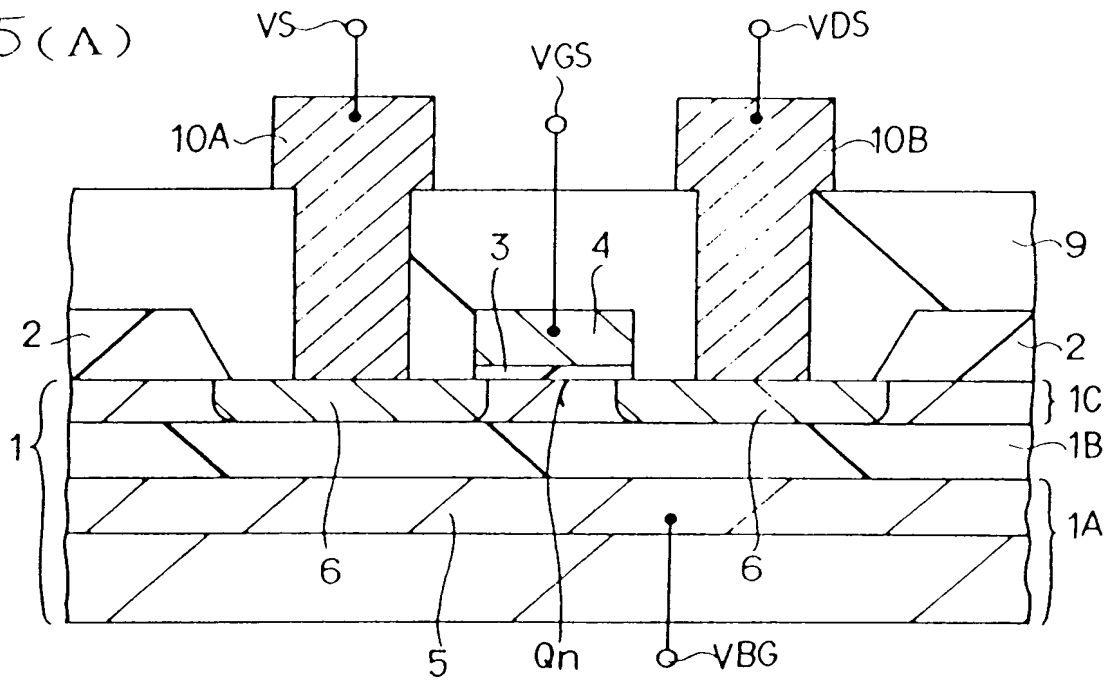


FIG 5(B)

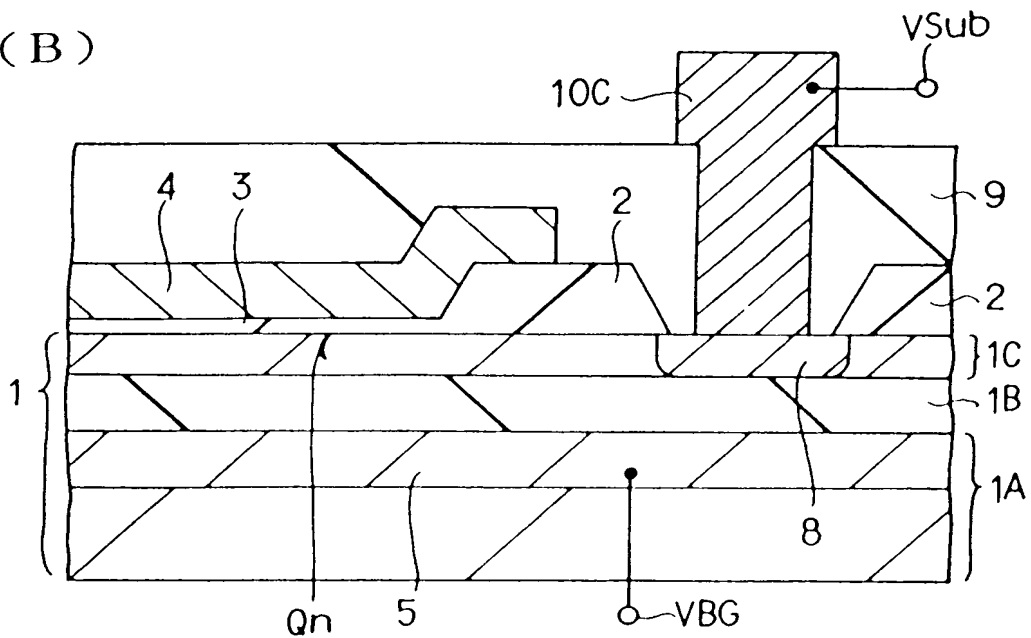


FIG. 10

FIG. 10(A)

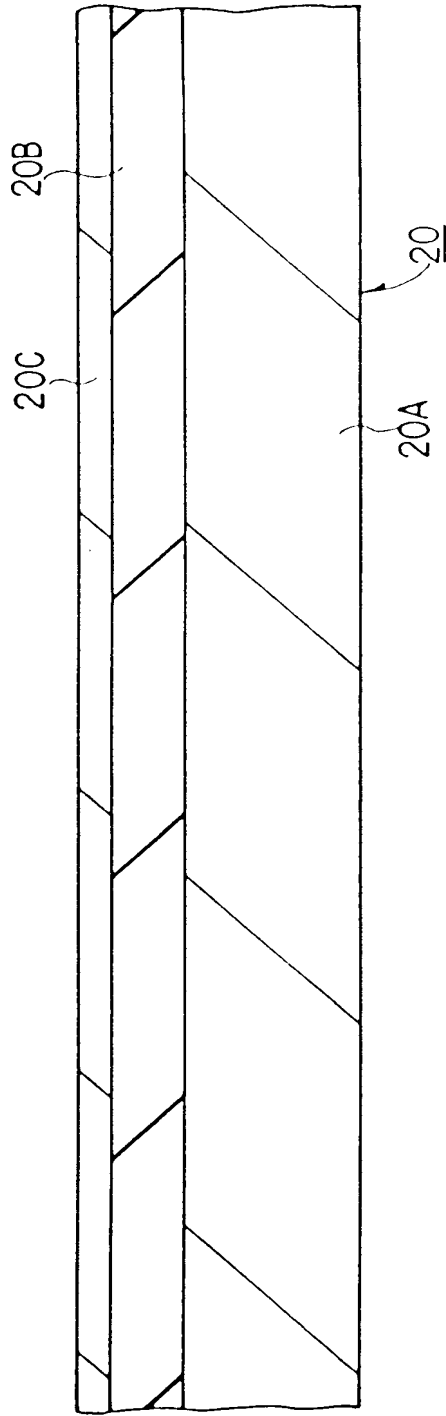


FIG. 10(B)

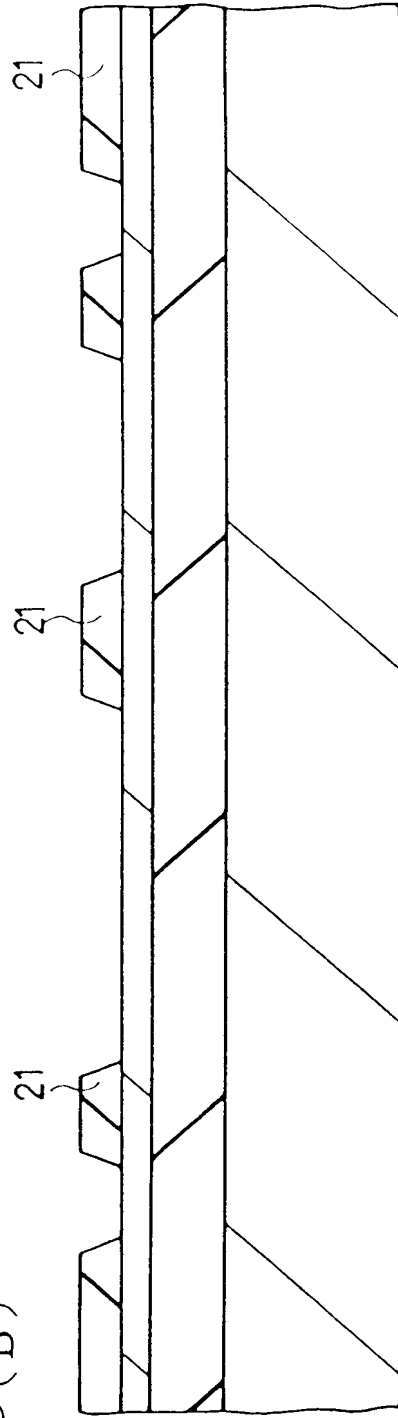
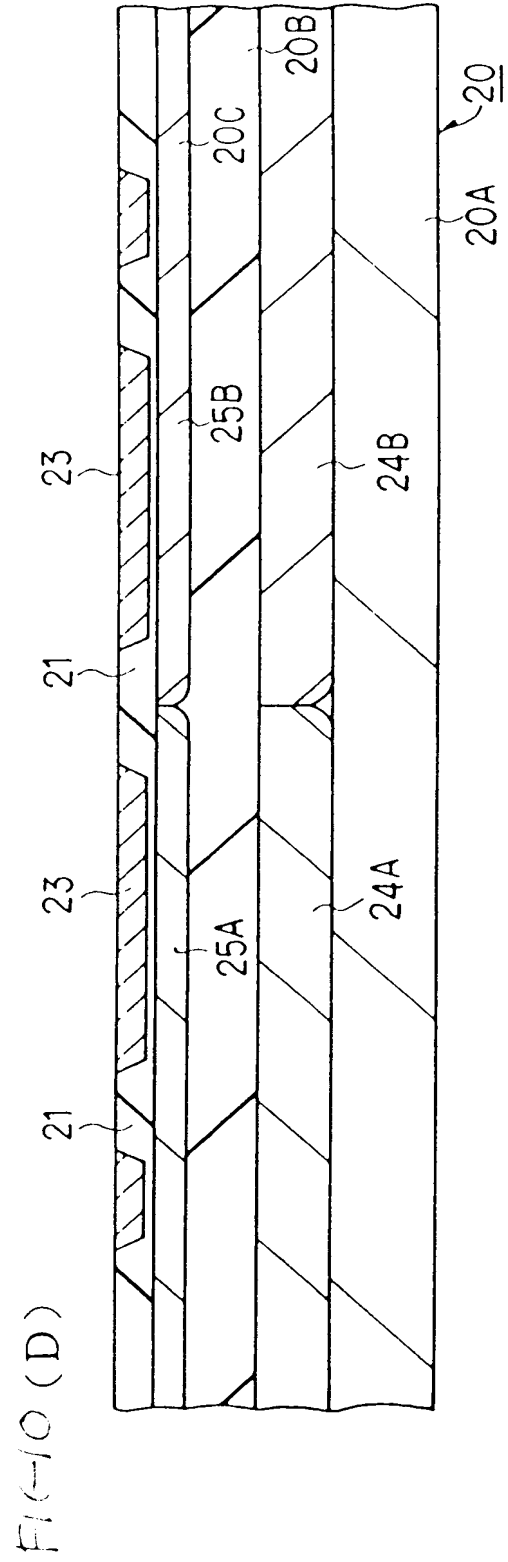
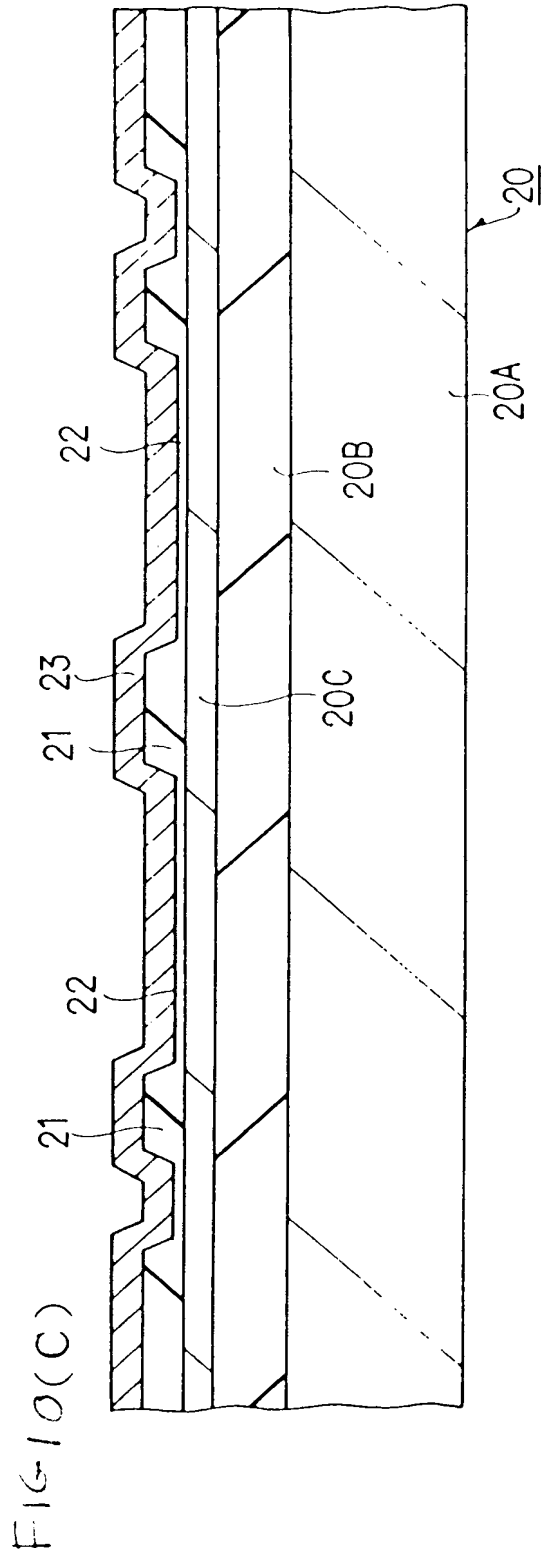


FIG. 11



25

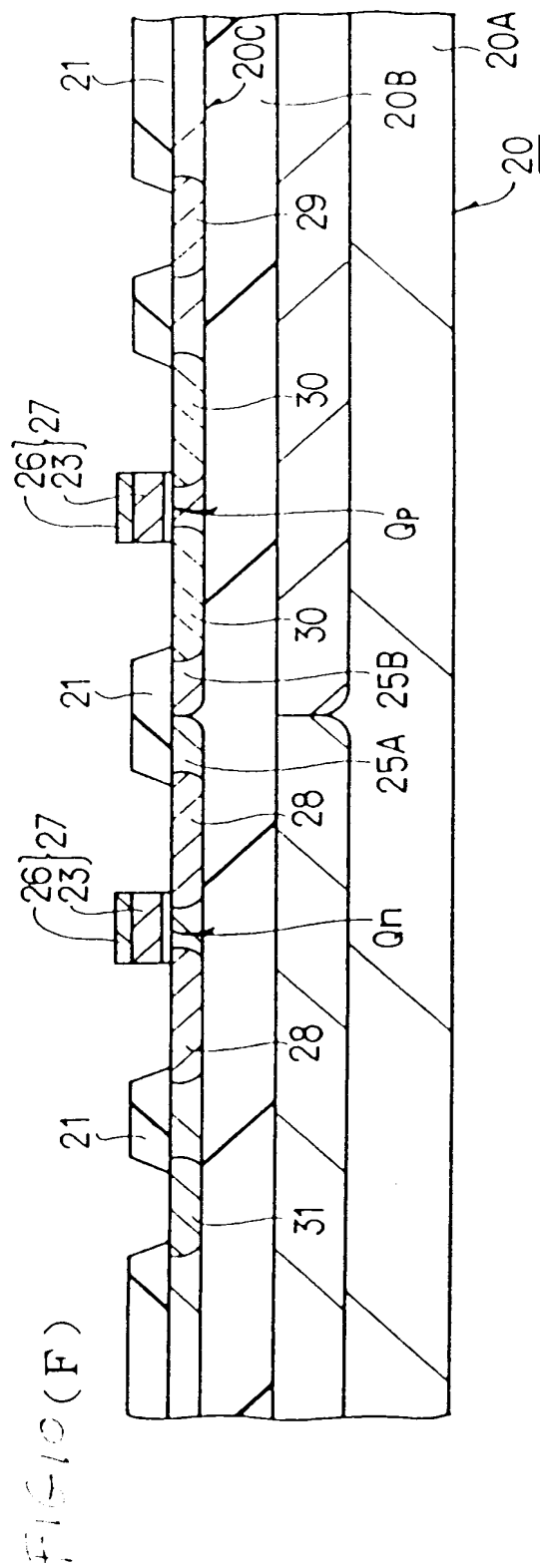
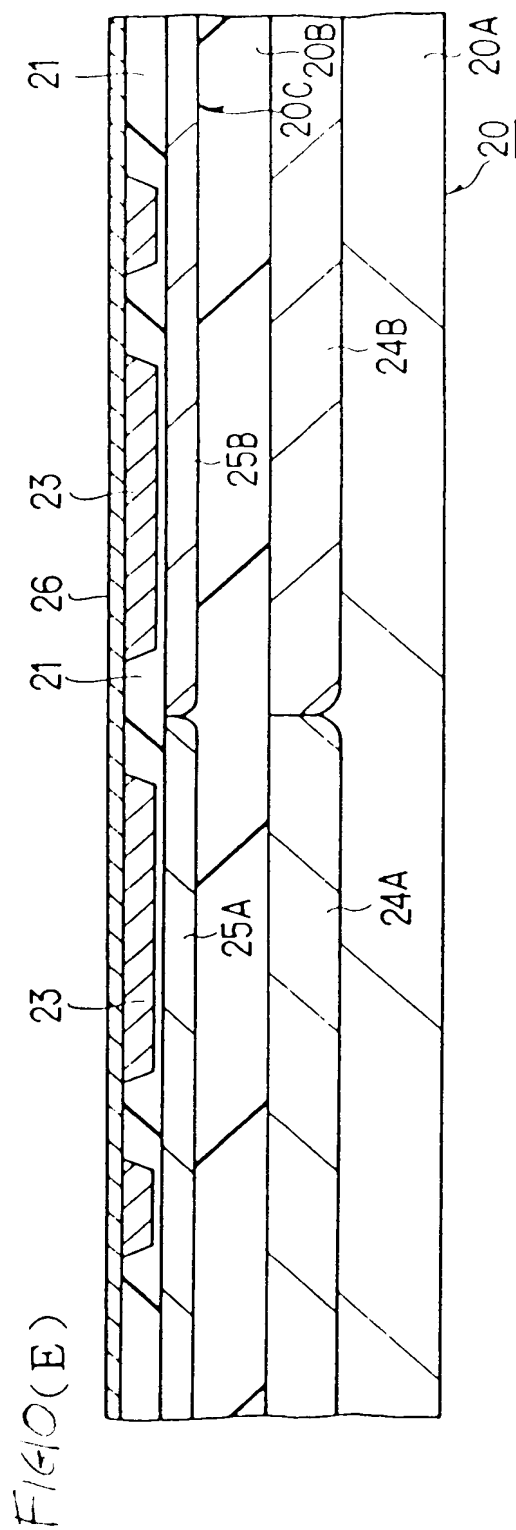


FIG. 11
~~FIG. 13~~

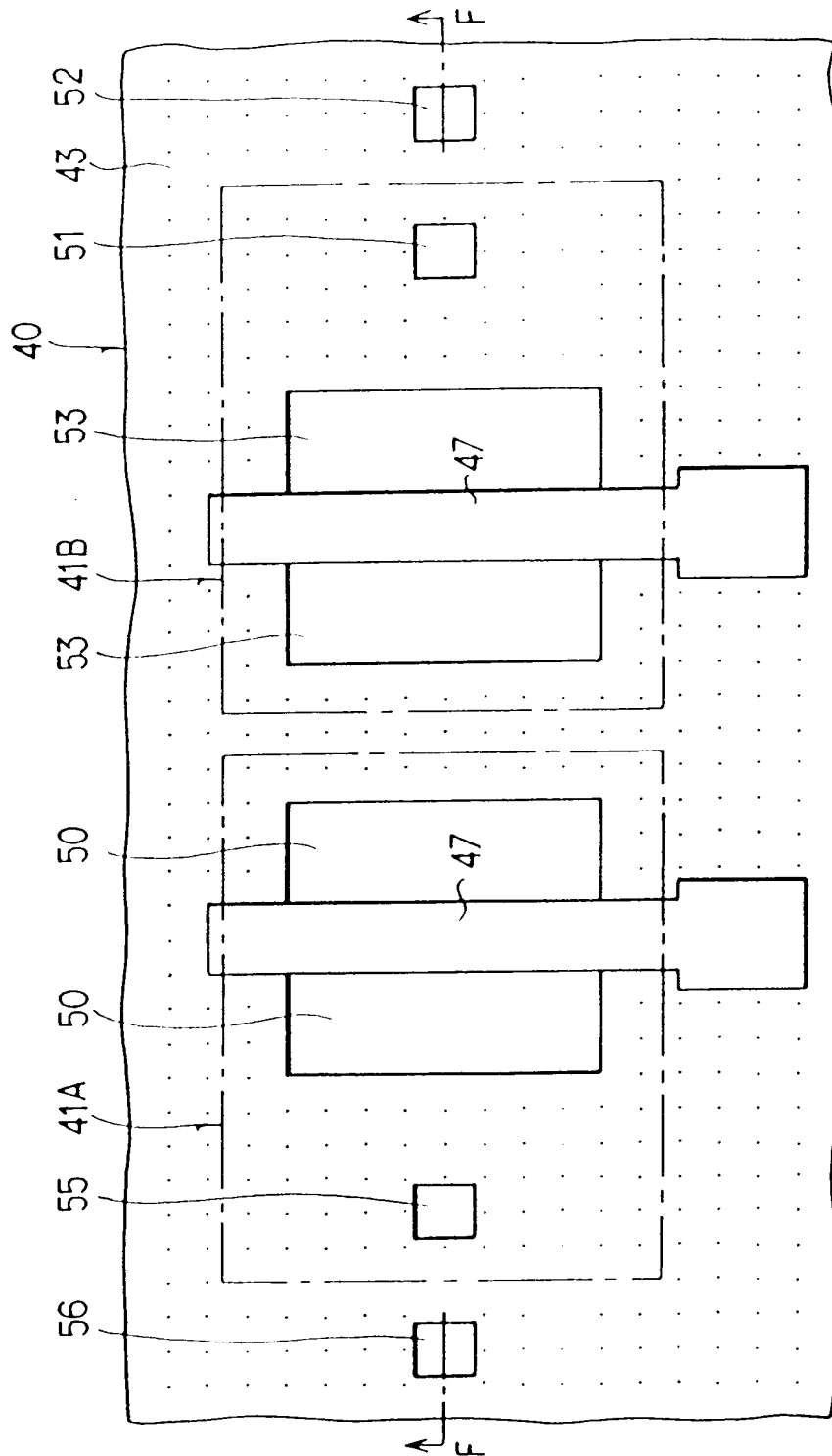


FIG. 12.
FIG. 14.

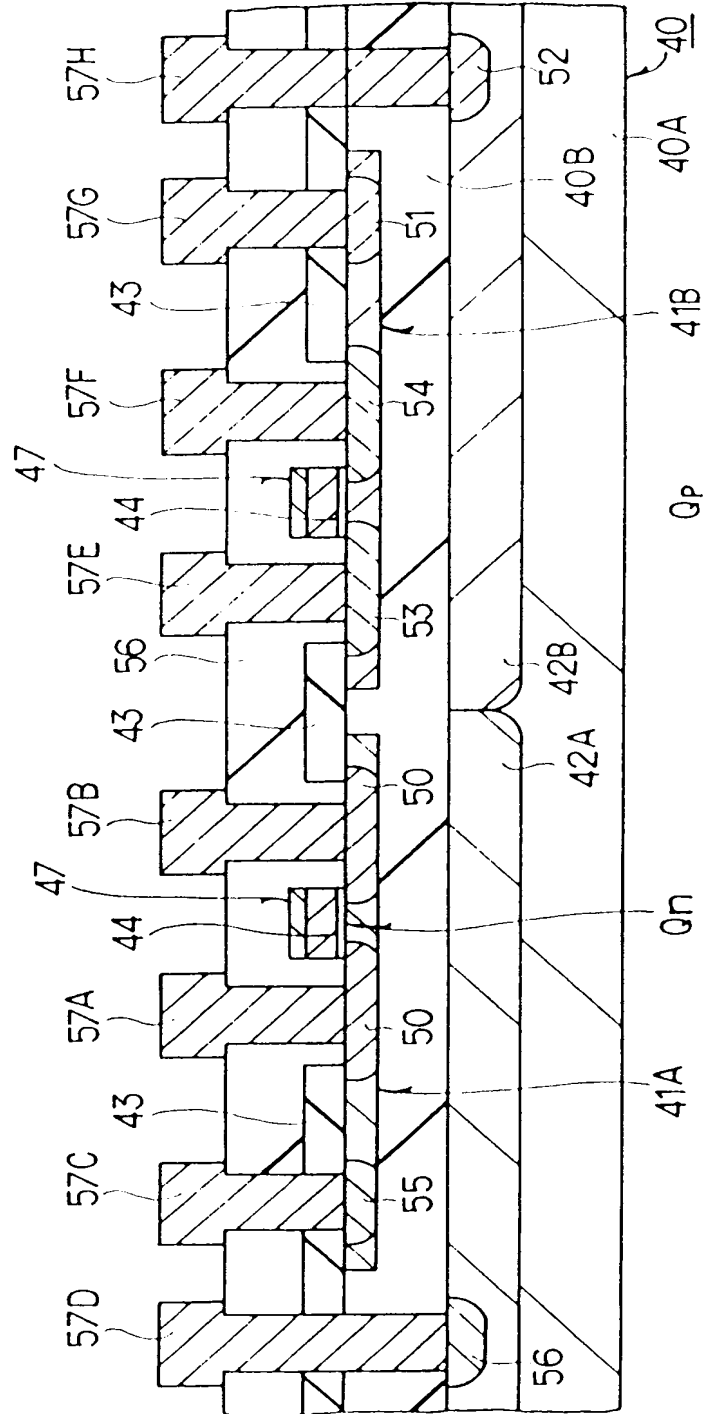


FIG. 15

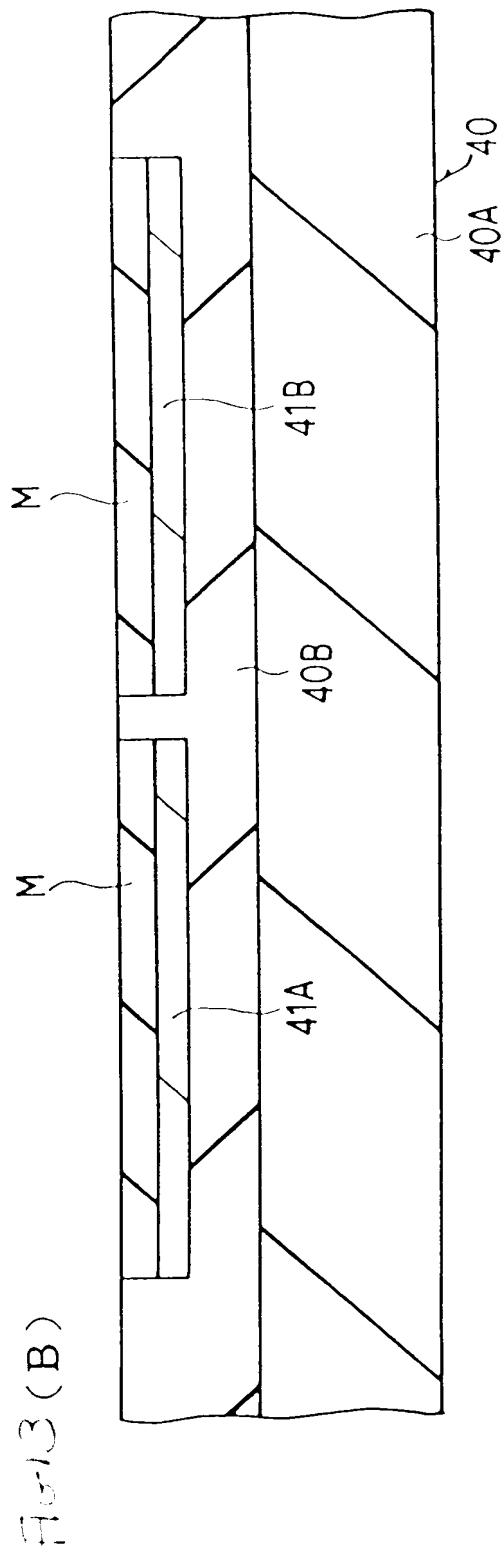
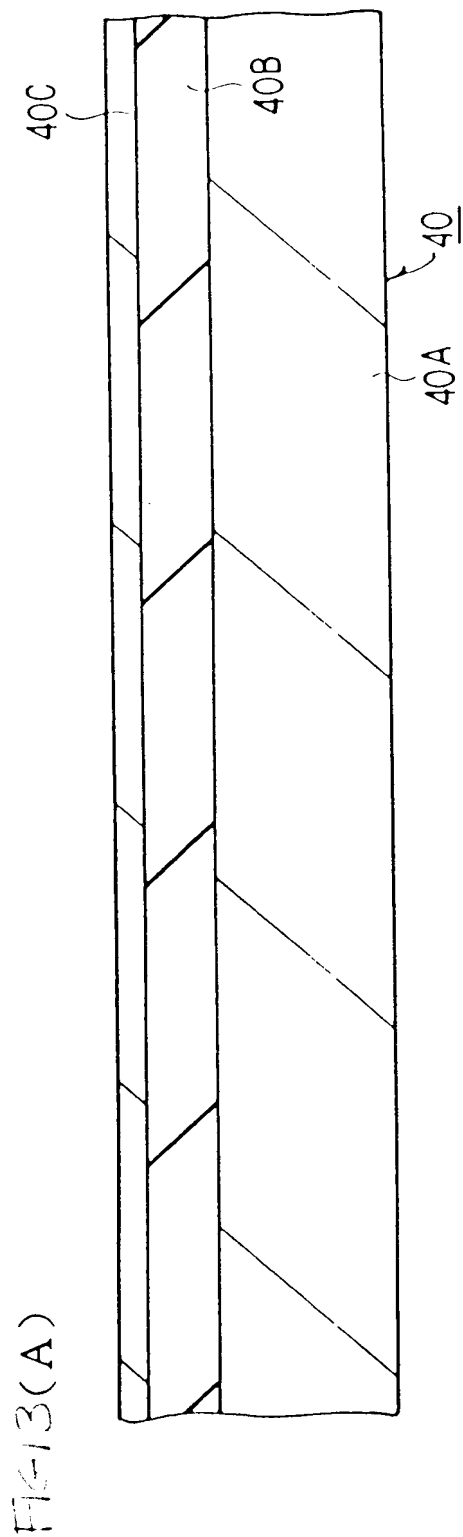


FIG. 10

FIG 13(C)

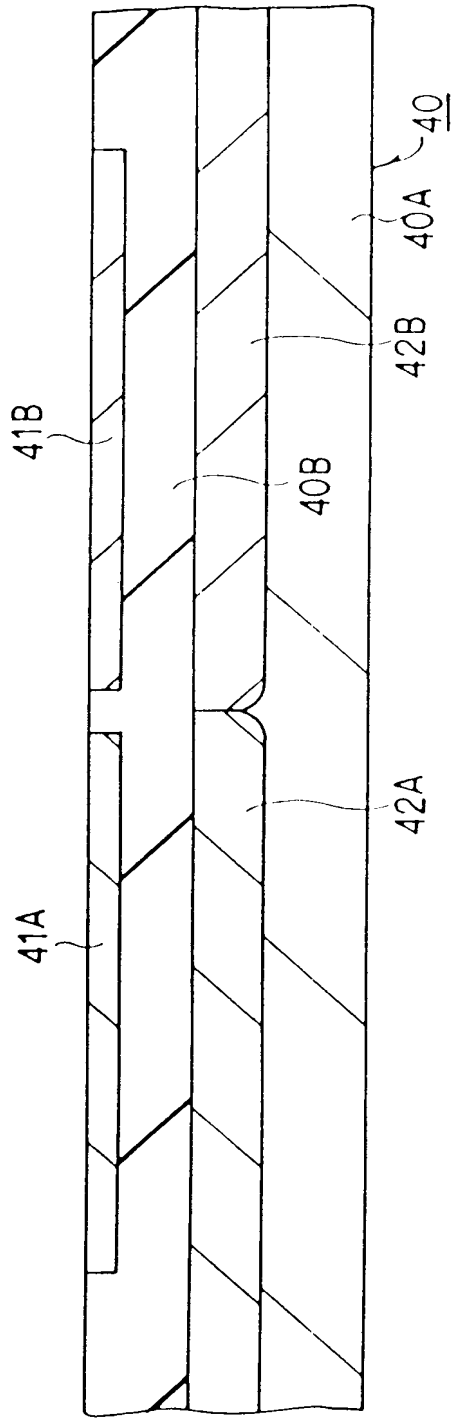


FIG 13(D)

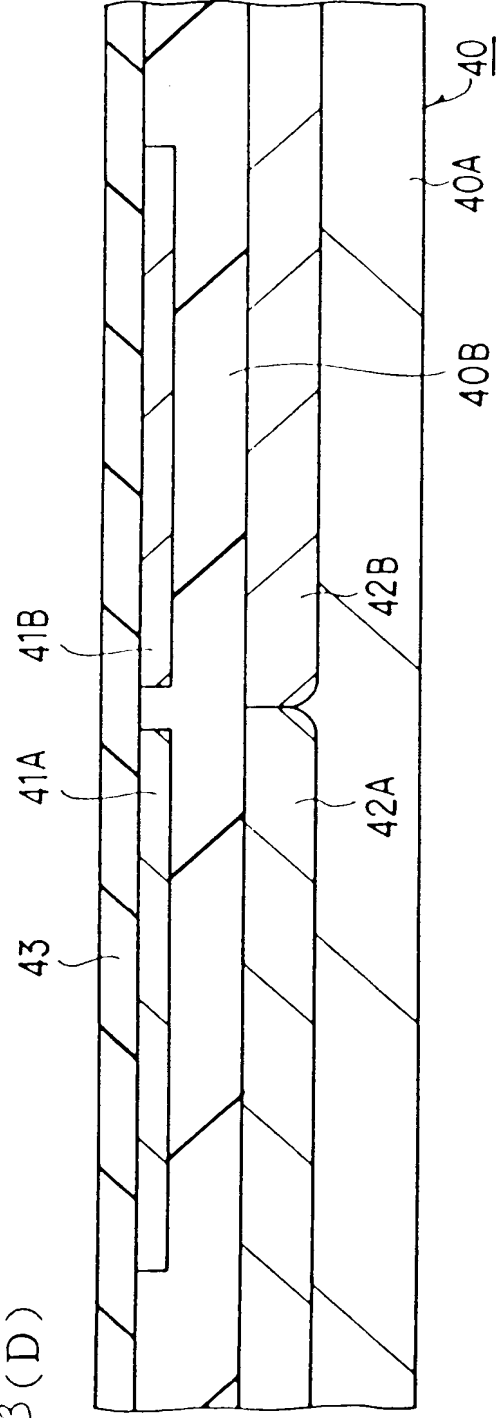


FIG. 17-

FIG. 13(E)

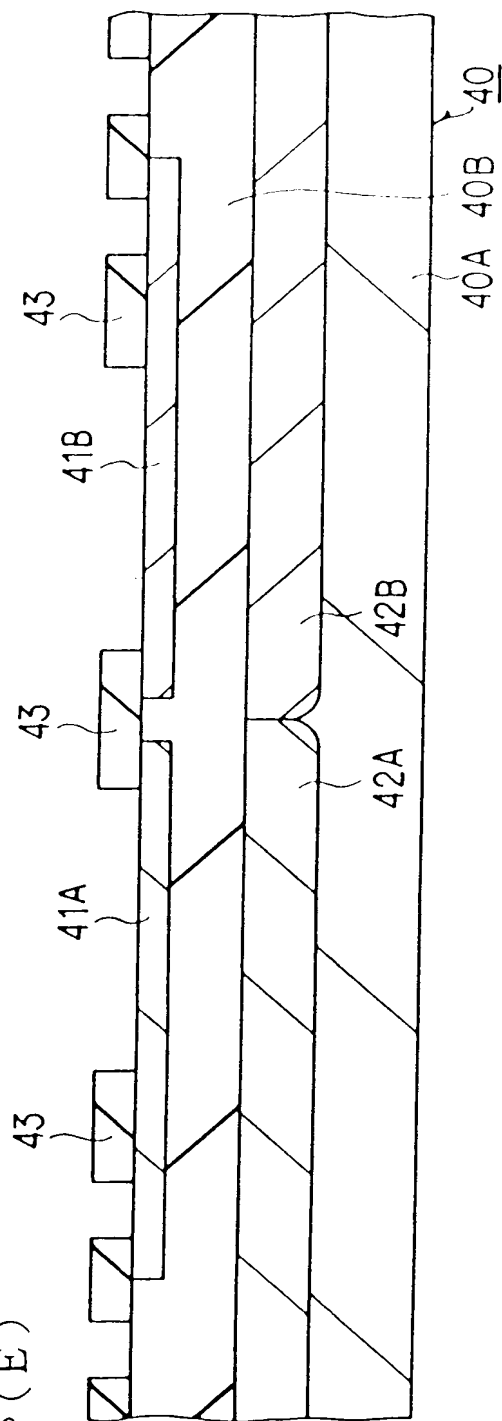


FIG. 13(F)

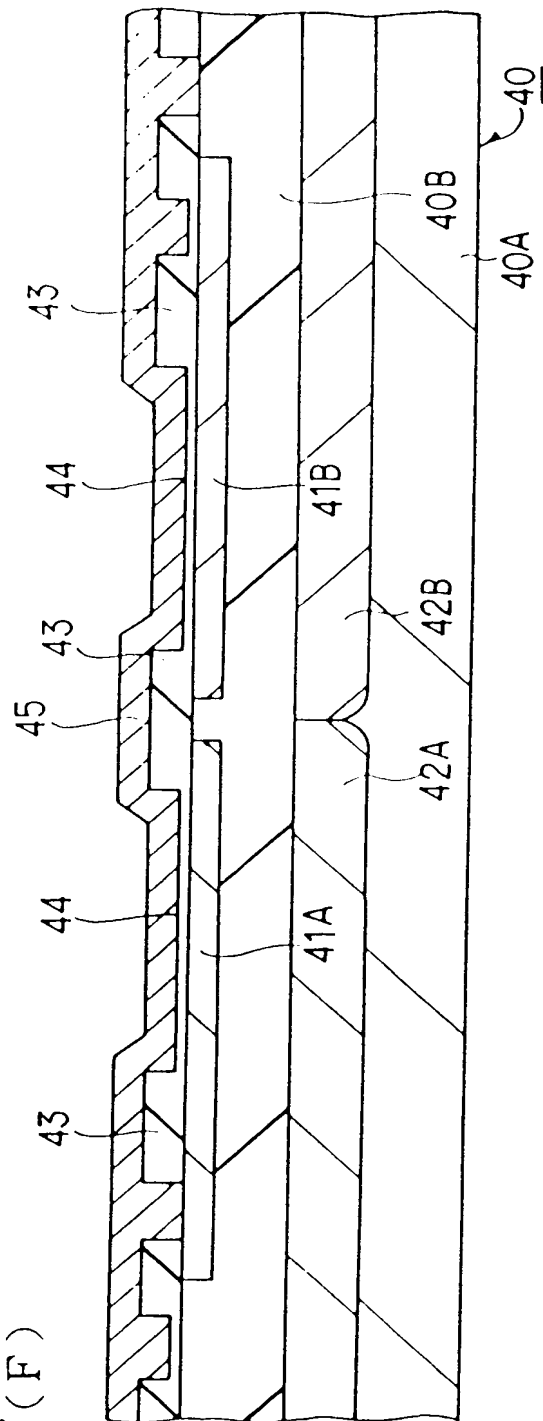


FIG. 18-

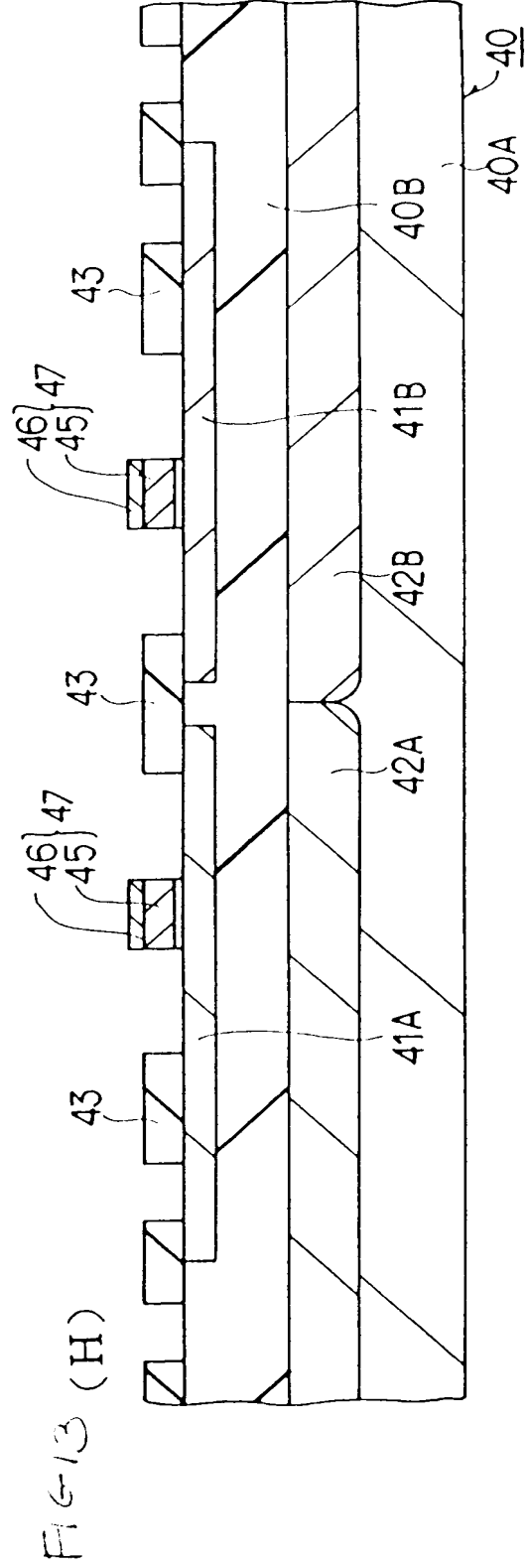
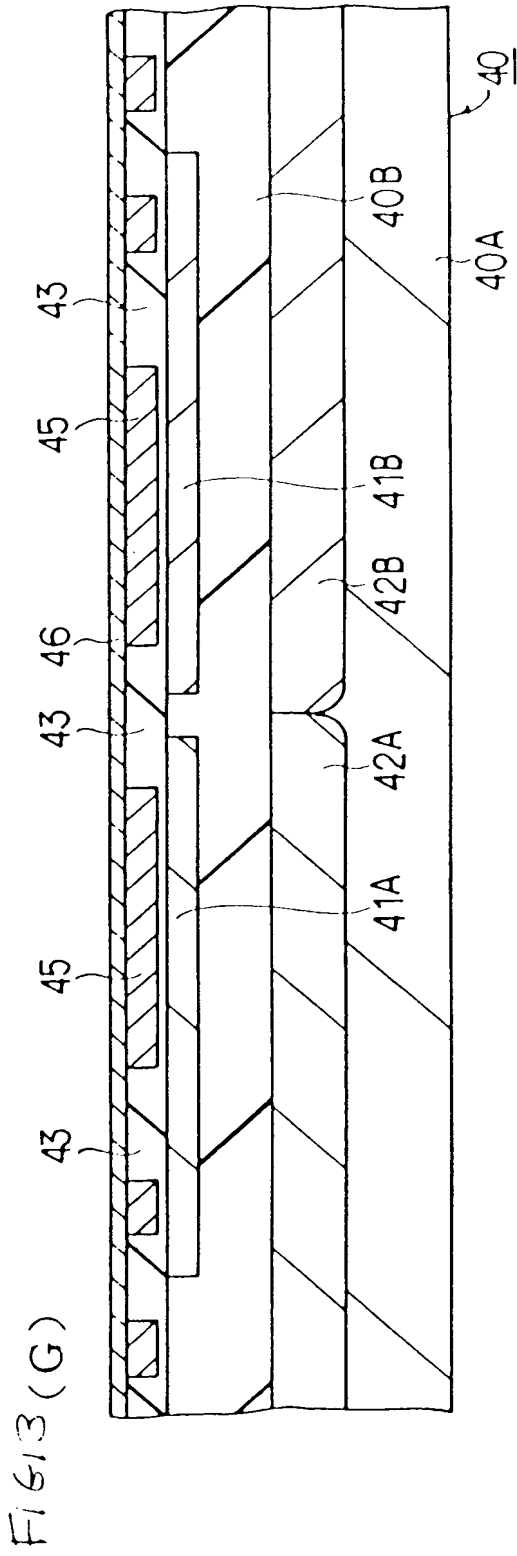


FIG. 19:-

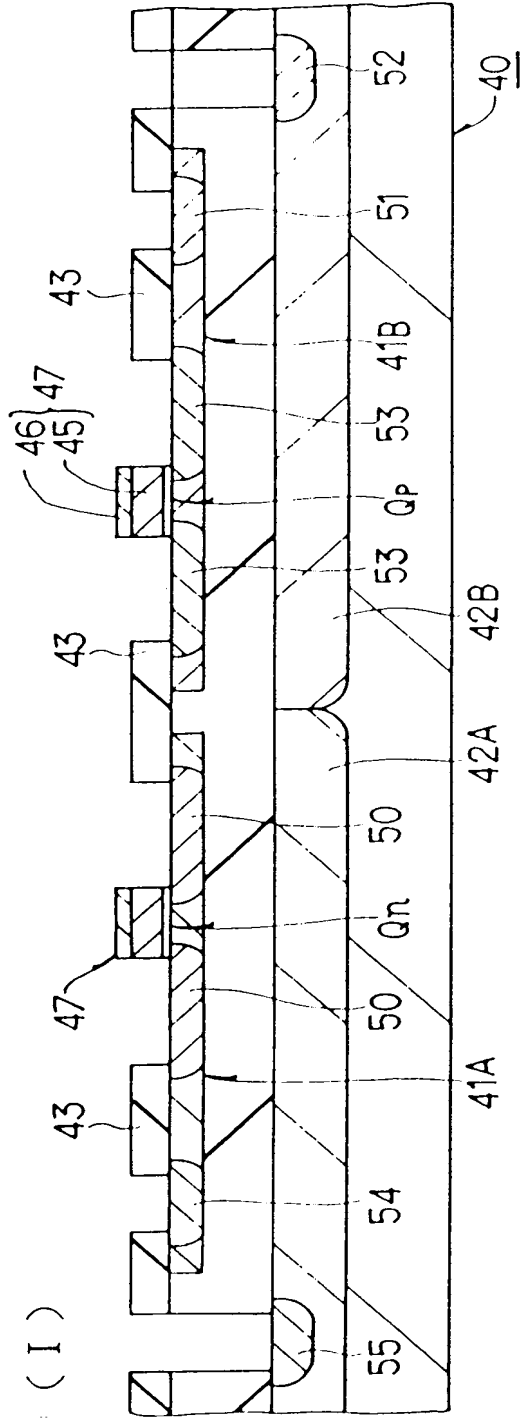
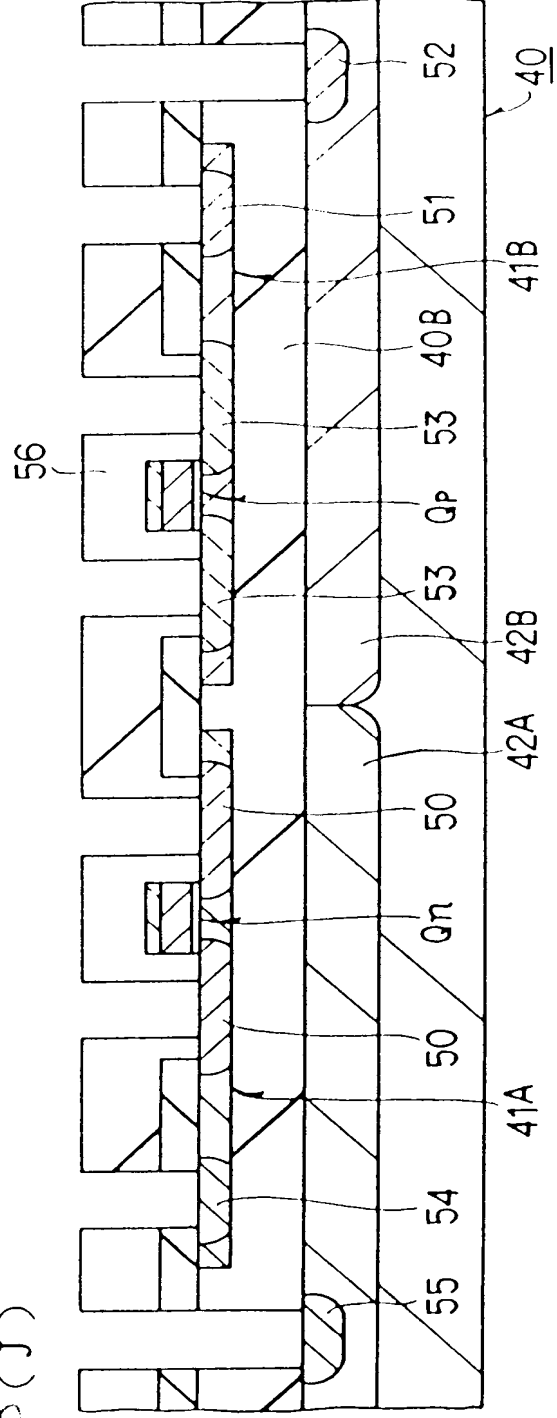


FIG. 13 (J)



156A
FIG. 21

(1) NORMAL OPERATION MODE

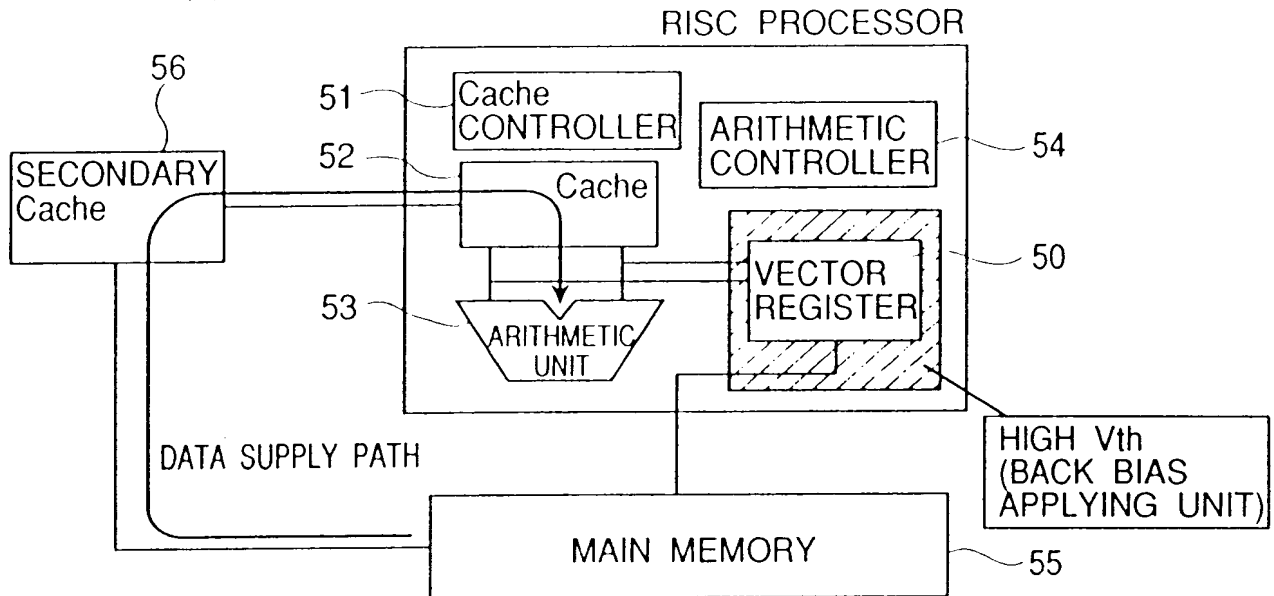


FIG 15(B)

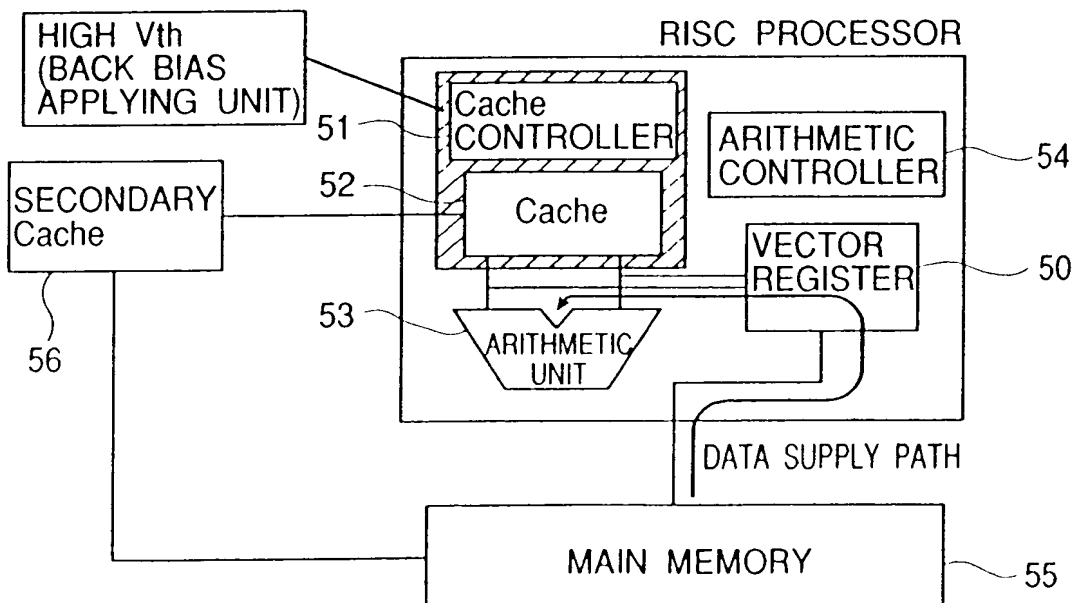
(2) MASS DATA NUMERICAL CALCULATION MODE
(VECTOR COMPUTE MODE)

FIG. 22

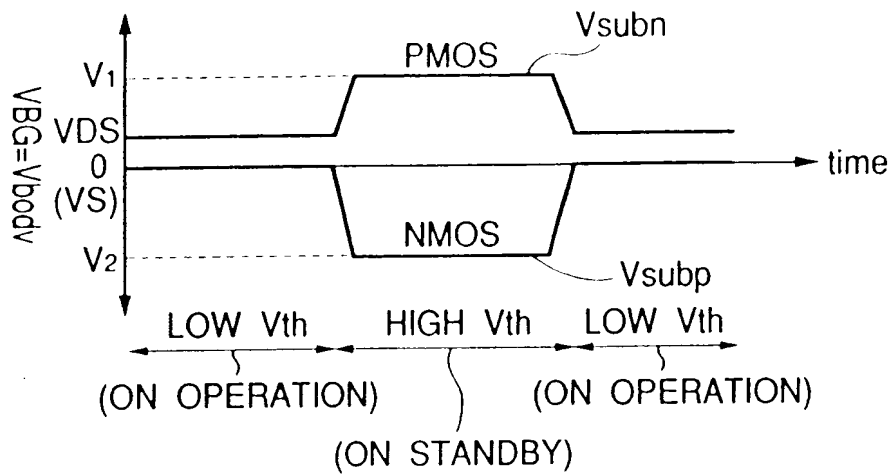


FIG. 23

